PhD / Post Doc positions in Smart Edge Processors

As the world witnesses the emergence of smart applications for smart applications powered by Artificial Intelligence (AI) in almost every edge device, there is an urgent need for ultra-low-power (ULP) edge AI System-on-Chips (SoC) or Smart Edge Processors (SEP) that offloads the computing closer to the source of data generation to address the limitations (e.g., latency, bandwidth) of cloud or centralized computing. However, this can only be realized if we can make SEPs at least 100 times more energy-efficient, while offering sufficient flexibility and scalability to deal with AI, which is a fast-moving target. Our EU-funded project **CONVOLVE** aims to achieve these targets by taking a holistic approach with innovations at all design stack levels, including memristive circuits, exploiting Compute-in-Memory (CIM) and approximate computing, advanced Deep Learning (DL) models, online learning, exploiting dynamism and reconfiguration at DL-, Architecture- and Circuit-levels, while rethinking the whole compiler stack.

We are looking for excellent, teamwork-oriented, and research-driven candidates with Computer Science, Electrical Engineering, or related background, with very strong software design skills, for joining as PhD and/or Post Doc candidates in any of the following research areas in **CONVOLVE** .

Ultra-low power CGRA for Dynamic ANNs and SNNs: Research and develop near-memory computing engines based on Coarse-Grained Reconfigurable Architectures (CGRA) using a flexible memory fabric for Dynamic Neural Networks supporting Artificial Neural Network (ANN) and brain-inspired Spiling Neural Network (SNN) models. These designs need to be equipped with self-healing mechanisms to (partly) recover in the event of failures, enhancing system-level reliability. The accelerators may also have knobs to exploit near-threshold and approximate computing for extreme energy-efficient operation. Explore new opportunities brought about by 3D stacked silicon integration to dynamically swap data and configuration associated with neural network regions/layers/neurons to/from memory layers and deliver low-latency flows of neural processing with minimal stall.

Compiler Design for Smart Edge Processors: Research and develop a high-quality compiler backend for CGRA targets supporting SNNs and ANNs. Compared to existing solutions, the energy efficiency needs to be improved by exploiting SIMD, memory hierarchy, reuse, sparsity, etc.

Compositional performance analysis and architecture Design Space Exploration (DSE): Research and develop an infrastructure to model energy & latency at the SoC level, including the SoC level memory hierarchy and processing host, as well as integrating the different accelerator component models. To support rapid evaluations needed for the DSE, analytical models need to be pursued. The development of compositional models will moreover enable run-time performance assessment of an application when the platform configuration changes due to a failing platform component.

Composable and Secure SoC accelerator platform: Research and develop novel composable and real-time design techniques to realize an ultra-low-power and real-time Trusted Execution Environment (TEE) for an SoC platform consisting of RISC-V cores with several accelerators. Different security features that protect against physical attacks need to be integrated into the SoC platform, while maintaining ultra-low-power and real-time requirements of the applications. The platform should allow easy integration of Post-Quantum Cryptography accelerators and CIM based hardware accelerators.

More information on the PhD/Post Doc positions can be found under the respective link below:

PhD positions: https://jobs.tue.nl/en/vacancy/phd-positions-on-seamless-design-of-smart-edge-processors-969138.html

Post-Doc positions: https://jobs.tue.nl/en/vacancy/postdoc-positions-on-seamless-design-of-smart-edge-processors-969136.html

Please contact dr.ir. Sander Stuijk, s.stuijk@tue.nl if you would like to more about the positions.